**TIMERS AND PHASE LOCKED LOOPS**

**INTRODUCTION TO 555 TIMER**

One of the most versatile linear integrated circuits is the *555* timer. A sample of these applications

includes mono-stable and astable multivibrators, dc-dc converters, digital logic probes, waveform generators,analog frequency meters and tachometers, temperature measurement and control, infrared transmitters, burglar and toxic gas alarms, voltage regulators, electric eyes, and many others.

The 555 is a monolithic timing circuit that can produce accurate and highly stable time delays or

oscillation. The timer basically operates in one of the two modes: either as monostable (one-shot)

multivibrator or as an astable (free running) multivibrator.The device is available as an 8-pin metal can, an 8-pin mini DIP, or a 14-pin DIP.

The SE555 is designed for the operating temperature range from -55°Cto + 125°C, while the NE555

operates over a temperature range of 0° to +70°C. The important features of the 555 timer are these: it

operates on +5 to + 18 V supply voltage in both free-running (astable) and one- shot (monostable) modes; it has an adjustable duty cycle; timing is from microseconds hrough hours; it has a high current output; it can source or sink 200 mA; the output can drive TTL and has a temperature stability of 50 parts per million (ppm) per degree Celsius change in temperature, or equivalently 0.005%/°C.

Like general-purpose op-amps, the 555 timer is reliable, easy to us, and low cost.

**Pin 1:** Ground. All voltages are measured with respect to this terminal.

**Pin 2:** Trigger. The output of the timer depends on the amplitude of the external trigger pulse applied to this pin. The output is low if the voltage at this pin is greater than 2/3 VCC. However,when a negative-going pulse of amplitude larger than 1/3 VCC is applied to this pin, the comparator 2 output goes low, which in turn switches the output of the timer high The output remains high as long as the trigger terminal is held at a low voltage.

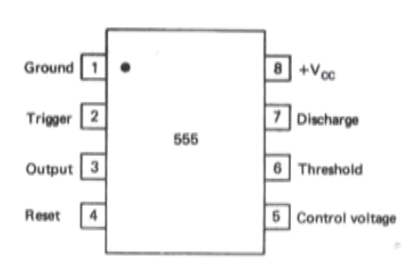
**Pin 3:** Output. There are two ways a load can be connected to the output terminal: either between pin 3and ground (pin 1) or between pin 3 and supply voltage + VCC (pin 8) . When the output is low, the load current flows through the load connected between pin 3 and + VCC into the output terminal and is called the sinkcurrent.

However, the current through the grounded load is zero when the output is low. For this reason, the

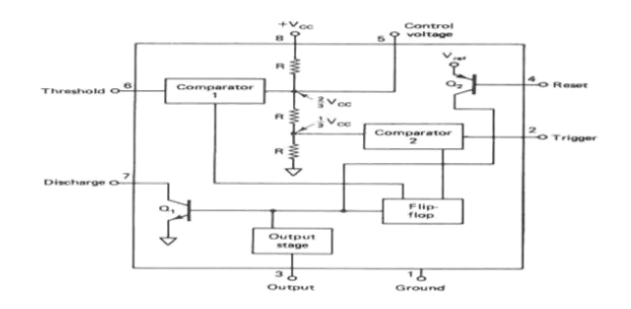
load connected between pin 3 and + VCC is called the normally on load and that connected between pin 3 and ground is called the normally off load.

On the other hand, when the output is high, the current through the load connected between pin 3and +

VCC (normally on load) is zero. However, the output terminal supplies current to the normally off load. This current is called the source current. The maximum value of sink or source current is 200 mA.



**Pin 4:** Reset. The 555 timer can be reset (disabled) by applying a negative pulse to this pin. When the reset function is not in use, the reset terminal should be connected to + VCC to avoid any possibility of false triggering.



Block Diagram

**Pin 5:** Control voltage. An external voltage applied to this terminal changes the threshold as well

as the trigger voltage . In other words, by imposing a voltage on this pin or by connecting a pot between this pin and ground, the pulse width of the output waveform can be varied. When not used, the control pin

should be bypassed to ground with a 0.01-µF capacitor to prevent any noise problems.

**Pin 6:** Threshold. This is the non-inverting input terminal of comparator 1, which monitors the voltage

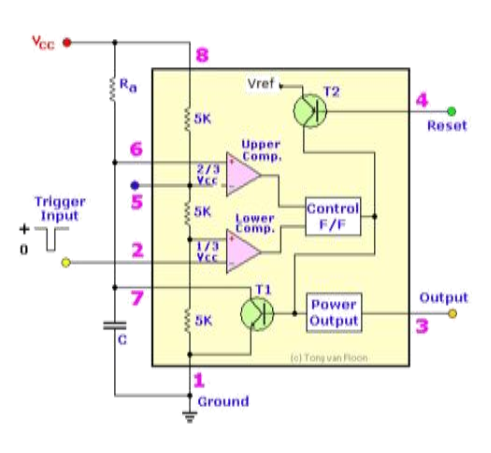
across the external capacitor . When the voltage at this pin is threshold voltage 2/3 V, the output of

comparator 1 goes high, which in turn switches the output of the timer low.

**Pin 7:** Discharge. This pin is connected internally to the collector of transistor Q1, as shown in Figure 4-1(b). When the output is high, Q1 is off and acts as an open circuit to the external capacitor C connected across it. On the other hand, when the output is low, Q1 is saturated and acts as a short circuit, shorting out the external capacitor C to ground.

**Pin 8:** + VCC. The supply voltage of +5 V to +18 is applied to this pin with respect to ground (pin 1).

**FUNCTIONAL BLOCK DIAGRAM OF 555 TIMER**



**THE 555 AS A MONOSTABLE MULTIVIBRATOR**

A monostable multivibrator, often called a one-shot multivibrator, is a pulse- generating circuit in

which the duration of the pulse is determined by the RC network connected externally to the 555 timer.

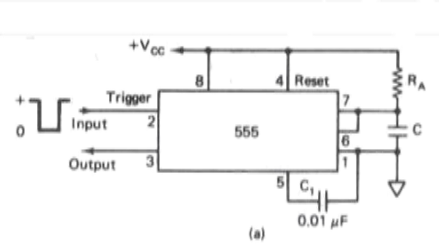
In a stable or standby state the output of the circuit is approximately zero or at logic-low level.

When an external trigger pulse is applied, the output is forced to go high ( ˜VCC). The time the output

remains high is determined by the external RC network connected to the timer. At the end of the timing

interval, the output automatically reverts back to its logic-low stable state. The output stays low until the

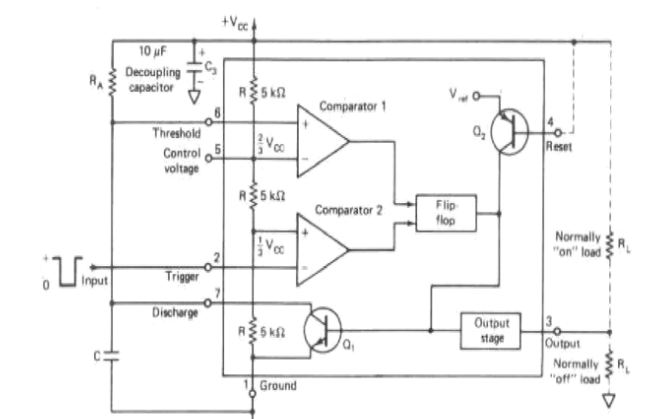
trigger pulse is again applied. Then the cycle repeats. The monostable circuit has only one stable state (output low), hence the name mono-stable.Normally, the output of the mono- stable multivibrator is low. Fig 4.2 (a) shows the 555 configured formonostable operation. To better explain the circuit’s operation



**Mono-stable operation:** According to Fig 4-2(b), initially when the output is low, that is, the circuit is in a stable state, transistor Q is on and capacitor C is shorted out to ground. However, upon application of a negative trigger pulse to pin 2, transistor Q is turned off, which releases the short circuit across the external capacitor C and drives the output high. The capacitorC now starts charging up toward Vcc through RA.

However, when the voltage across the capacitor equals 2/3 Va., comparator I ‘s output switches

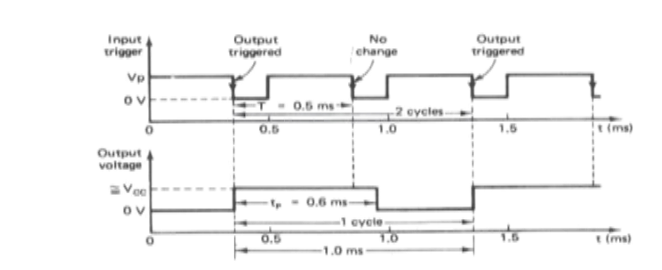
from low to high, which in turn drives the output to its low state via the output of the flip-flop. At the same time, the output of the flip-flop turns transistor Q on, and hence capacitor C rapidly discharges through the transistor. The output of the rnonostable remains low until a trigger pulse is again applied. Then the cycle repeats. Figure 4-2(c) shows the trigger input, output voltage, and capacitor voltage waveforms. As shownhere, the pulse width of the trigger input must be smaller than the expected pulse width of the output waveform. Also, the trigger pulse must be a negative-going input signal with amplitude larger than 1/3 the time during which the output remains high is given by where



where RA is in ohms and C is in farads. Figure 4-2(c) shows a graph of the various combinations of RA and C necessary to produce desired time delays. Note that this graph can only be used as a guideline and gives only the approximate value of RA and C for a given time delay. Once triggered, the circuit’s output will remain in the high state until the set time 1, elapses. The output will not change its state even if an input trigger is applied again during this time interval T. However, the circuit can be reset during the timing cycle by applying a negative pulse to the reset terminal. The output will then remain in the low state until a trigger is again applied. Often in practice a decoupling capacitor (10 F) is used between + (pin 8) and ground (pin 1) to eliminate unwanted voltage spikes in the output waveform. Sometimes, to prevent any possibility of mistriggering the monostable multivibrator on positive pulse edges, a wave shapingcircuit consisting of R, C2, and diode D is connected between the trigger input pin 2 and pin 8, as shown in Figure 4-3. The values of R and C2 should be selected so that the time constant RC2 is smaller than the output pulse width.

**Monostable Multivibrator Applications**

1. **Frequency divider:** The monostable multivibrator of Figure 4-2(a) can be used as a frequency divider by adjusting the length of the timing cycle tp, with respect to the tine period T of the trigger input signal applied to pin 2. To use monostable multivibrator as a divide-by-2 circuit, the timing interval tp must be slightly larger than the time period T of the trigger input signal, as shown in Figure 4-4. By the same concept, to use the monostable multivibrator as a divide-by-3 circuit, tp must be slightly larger than twice the period of the input trigger signal, and so on. The frequency-divider application is possible because the monostable multivibrator cannot betriggered during the timing cycle.



**Pulse stretcher:** This application makes use of the fact that the output pulse width (timing interval) of

the rnonostable multivibrator is of longer duration than the negative pulse width of the input trigger. As

such, the output pulse width of the monostable multivibrator can be viewed as a stretched version of the

narrow input pulse, hence the name pulse stretcher. Often, narrow-pulse- width signals are not suitable for

driving an LED display, mainly because of their very narrow pulse widths. In other words, the LED may be flashing but is not visible to the eye because its on time is infinitesimally small compared to its off time. The 555 pulse stretcher can be used to remedy this problem

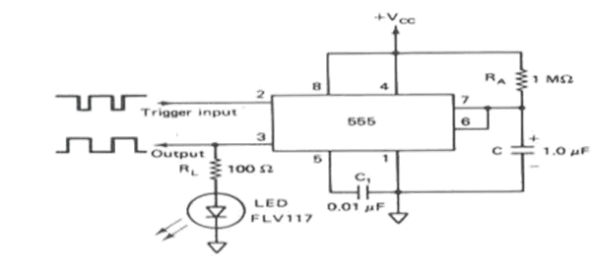


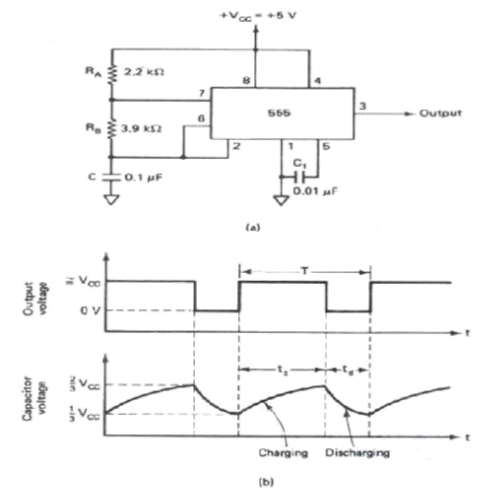
Figure 4-5 shows a basic rnonostable used as a pulse stretcher with an LED indicator at the output.

The LED will be on during the timing interval tp = 1.1RAC, which can be varied by changing the value of

RA and/or C.

**THE 555 AS AN ASTABLE MULTIVIBRATOR**

The 555 as an Astable Multivibrator, often called a free-running multivibrator, is a rectangular-wavegenerating circuit. Unlike the monostable multivibrator, this circuit doesNot require an external trigger to change the state of the output, hence the name freerunning. However, the time during which the output is either high or low is determined by the two resistors and a capacitor, which are externally connected to the 555 timer. Fig 46(a)shows the 555 timer connected as an astable multivibrator. Initially, when the output is high, capacitor C starts charging toward V through RA and R8. However as soon as voltage across the capacitor equals 2/3 Vcc, comparator I triggers the flip flop, and the output switches low [see Fig 4-6(b)]. Now capacitor C starts discharging through R8 and transistor Q. When the voltage across C equals 1/3 comparator 2’s output triggers the flip-flop, and the output goes high. Then the cycle repeats.



The output voltage and capacitor voltage waveforms are shown in Figure 4-6(b). As shown in this

figure, the capacitor is periodically charged and discharged between 2/3 Vcc and 1/3 V, respectively. The

time during which the capacitor charges from 1/3 V to 2/3 V. is equal to the time the output is high and is

given by

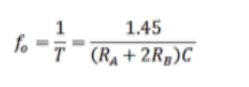


where RA and R3 are in ohms and C is in farads. Similarly, the time during which the capacitor

discharges from 2/3 V to 1/3 V is equal to the time the output is low and is given by

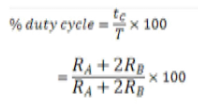
where RB is in ohms and C is in farads. Thus the total period of the output waveform is





Above equation indicates that the frequency fo is independent of the supply voltage V. Often the

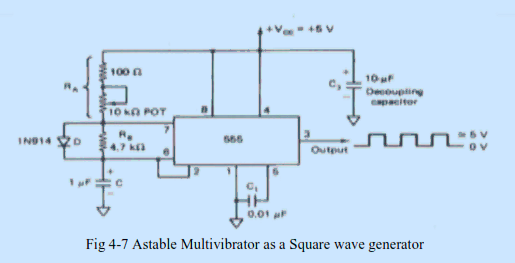
term duty cycle is used in conjunction with the astable multivibrator . The duty cycle is the ratio of the time t during which the output is high to the total time period T. It is generally expressed as a percentage. In equation form,



**Astable Multivibrator Applications:**

**Square-wave oscillator:** Without reducing RA= 0 , the astable multivibrator can be used to

producea square wave output simply by connecting diode D across resistor RB, as shown in Figure 4-7. The capacitor C charges through RA and diode D to approximately 2/3 Vcc and discharges through RB and terminal 7 until the capacitor voltage equals approximately 1/3 Vcc;



then the cycle repeats. To obtain a square wave output (50% duty cycle), RA must be a combination of a

fixed resistor and potentiometer so that the potentiorneter can be adjusted for the exact square wave.

Free-running ramp generator: The asab1e multivibrator can be used as a free-running ramp generator when resistors RA and R3 are replaced by a current mirror. Figure 4-8(a) shows an astable

multivibrator configured to perform this function. The current mirror starts charging capacitor C toward Vcc at a constant rate.

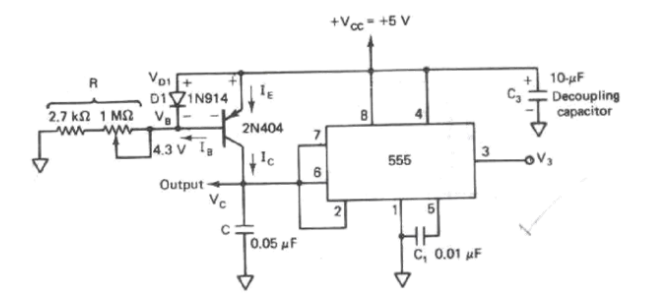
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multivibrator configured to perform this function. The current mirror starts charging capacitor C toward Vcc at a constant rate. When voltage across C equals 2/3 Vcc, comparator 1 turns transistor Q on, and C rapidly discharges through transistor Q. However, when the discharge voltage across C is approximately equal to 1/3 Vcc,omparator 2 switches transistor Q off, and then capacitor C starts charging up again. Thus the charge— discharge cycle keeps repeating. The discharging time of the capacitor is relatively negligible compared to its charging time; hence, for all practical purposes, the time period of the ramp waveform is equal to the charging time .







**PHASE-LOCKED LOOPS**

**Introduction**

The phase-locked loop principle has been used in applications such as FM (frequency modulation) stereo

decoders, motor speed controls, tracking filters, frequency synthesized transmitters and receivers, FM

demodulators, frequency shift keying (FSK) decoders, and a generation of local oscillator frequencies in

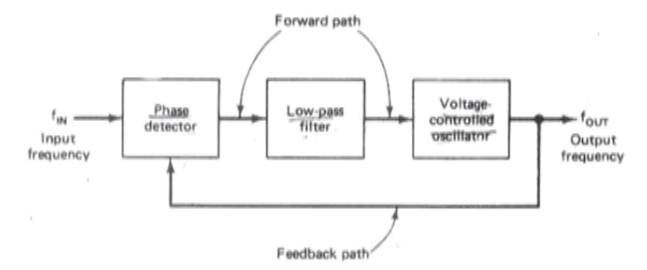
TV and in FM tuners. Today the phase-locked loop is even available as a single package, typical examples of which include the Signetics SE/NE 560 series (the 560, 561, 562, 564, 565, and 567). However, for more economical operation, discrete ICs can be used to construct a phase-locked loop.

**Bloch Schematic and Operating Principle**

Figure 4-10 shows the phase-locked loop (PLL) in its basic form. As illustrated in this figure,

the phase-locked loop consists of (1) a phase detector, (2) a low-pass filter, and, (3) a voltage

controlled oscillator.



The phase detectors or comparator compares the input frequency *f*IN with the feedback frequency

*f*OUT..The output voltage of the phase detector is a dc voltage and therefore is often referred to as the error

voltage. The output of the phase is then applied to the low-pass filter, which removes the high-frequency

noise and produces a dc level.

This dc level, in turn, is the input to the voltage-controlled oscillator (VCO). The filter also helps in

establishing the dynamic characteristics of the PLL circuit. The output frequency of the VCO is directly

proportional to the input dc level. The VCO frequency is compared with the input frequencies and adjusted until it is equal to the input frequencies. In short, the phase-locked loop goes through three states: freerunning, capture, and phase lock. Before the input is applied, the phase-locked loop is in the free-running state. Once the input frequency is applied, the VCO frequency starts to change and the phase-locked loop is said to be in the capture mode. The VCO frequency continues to change until it equals the input frequency, and the phaselocked loop is then in the phase-locked state. When phase locked, the loop

tracks any change in the input frequency through its repetitive action.

Before studying the specialized phase-locked-loop IC, we shall consider the discrete phaselocked

loop, which may be assembled by combining a phase detector, a low-pass filter, and a voltage-controlled

oscillator.

**(a) Phase detector:**

The phase detector compares the input frequency and the VCO frequency and generates a dc

voltage that is proportional to the phase difference between the two frequencies. Depending on the analog or

digital phase detector used, the PLL is either called an analog or digital type, respectively. Even though

most of the monolithic PLL integrated circuits use analog phase detectors, the majority of discrete phase

detectors in use are of the digital type mainly because of its simplicity.

A double-balanced mixer is a classic example of an analog phase detector. On the other

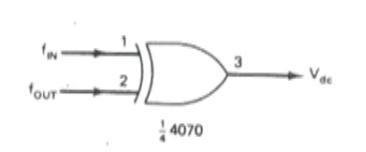
hand,examples of digital phase detectors are these:

1. Exclusive-OR phase detector

2. Edge-triggered phase detector

3. Monolithic phase detector (such as type 4044)

The following fig 4.11 shows Exclusive-OR phase detector:



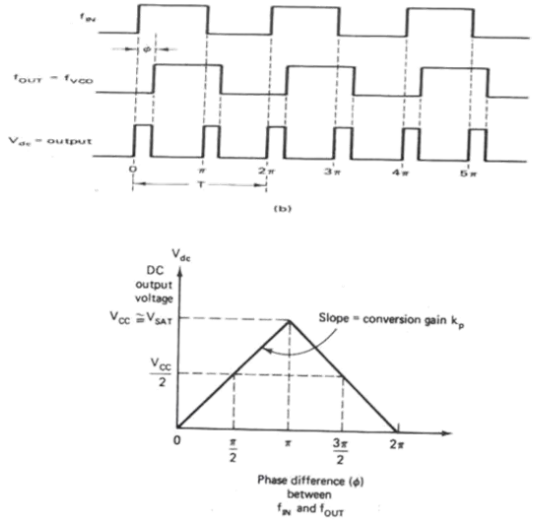


Fig 4-11(a) Exclusive-OR phase detector: connection and logic diagram. (b) Input and output waveforms.

(c) Average output voltage versus phase difference between *f*IN and *f*OUT curve.

**(b) Low-pass filter.**

The second block shown in the PLL block diagram of Figure 4-10 is a low-pass filter. The function

of the low-pass filter is to remove the high-frequency components in the output of the phase detector and to remove high-frequency noise.

More important, the 1ow-pass filter controls the dynamic characteristics of the phase-locked loop.

These characteristics include capture and lock ranges, bandwidth, and transient response. The lock range is defined as the range of frequencies over which the PLL system follows the changes in the input frequency. *f*IN. An equivalent term for lock range is tracking range. On the other hand, the capture range is the

frequency range in which the PLL acquires phase lock. Obviously, the capture range is always smaller

than the lock range.

**(c) Voltage-controlled oscillator:**

A third section of the PLL is the voltage-controlled oscillator.The VCO generates an output

frequency that is directly proportional to its input voltage.Typical example of VCO is Signetics NE/SE 566VCO, which provides simultaneous square wave and triangular wave outputs as a function of input voltage .The block diagram of the VCO is shown in Fig 4.12. The frequency of oscillations is determined by thee external R1 and capacitor C1 and the voltage VC applied to the control terminal 5.

The triangular wave is generated by alternatively charging the external capacitor C1 by one current source and then linearly discharging it by another. The charging and discharging levels are determined by Schmitt trigger action. The schmitt trigger also provides square wave output. Both the wave forms are buffered so that the output impedance of each is 50 ohms.

Fig 4.12 (c) is a typical connection diagram. In this arrangement the R1C1 combination determines

the free running frequency and the control voltage VC at pin 5 is set by voltage divider formed with R2 and

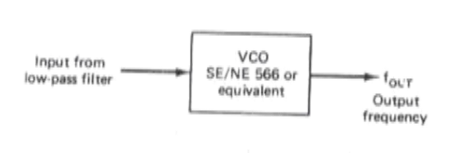
R3. The initial voltage VC at pin 5 must be in the range





where R1should be in the range 2KO < R1< 20KO. For affixed VC and constant C1, the frequency fO can

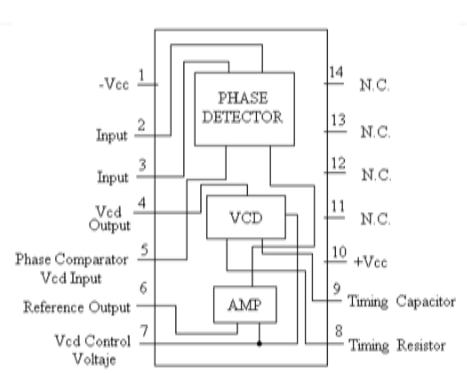
be varied over a 10:1 frequency range by the choice of R1 between 2KO < R1< 20KO.



**MONOLITHIC PHASE LOCK LOOPS IC 565:**

Monolithic PLLs are introduced by signetics as SE/NE 560 series and by national semiconductors LM

560 series.



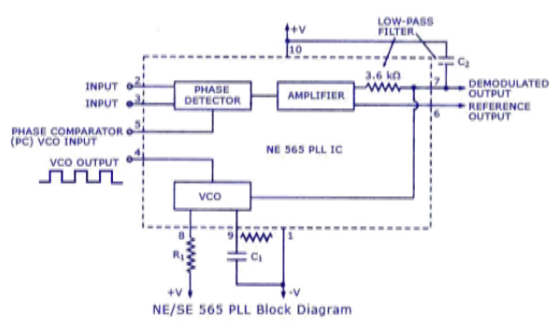


Fig 4.13 and 4.14 shows the pin diagram and block diagram of IC 565 PLL. It consists of phase

detector,amplifier,low pass filter and VCO.As shown in the block diagram the phase locked feedback loop is not internally connected.Therefore,it is necessary to connect out put of VCO to the phase comparator input,externally.In frequency multiplication applications a digital frequency divider is inserted into the loop i.e between pin 4 and pin 5.

The centre frequency of the PLL is determined by the free-running frequency of the VCO and it

is given by



Where R1 and C1 are an external resistor and capacitor connected to pins 8 and 9, respectively.The

values of R1 and C1 are adjusted such that the free running frequency will be at the centre of the input

frequency range.The values of R1 are restricted from 2 kΩ to 20 kΩ,but a capacitor can have any value.A

capacitor C2 connected between pin 7 and the positive supply forms a first order low pass filter with an

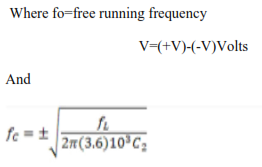
internal resistance of 3.6 kΩ.The value of filter capacitor C2 should be larger enough to eliminate possible

demodulated output voltage at pin 7 in order to stabilize the VCO frequency

The PLL can lock to and track an input signal over typically ±60% bandwidth w.r.t fo as the center

frequency. The lock range fL and the capture range fC of the PLL are given by the following equations.

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From above equation the lock range increases with an increase in input voltage but decrease with

increase in supply voltage.The two inputs to the phase detector allows direct coupling of an input

signal,provided that there is no dc voltage difference between the pins and the dc resistances seen from

pins 2 and 3 are equal.